REMARKS

Applicant concurrently files herewith a Request for Continued Examination and a petition and fee for a one month extension of time.

Claims 1, 5-9, 11-13, 30, 35, 37, and 38 are presently pending in this application. Claims 5, 11-13, 30, 35, 37, and 38 have been amended to more particularly define the invention. Claims 2, 4, 10, 22-29, 31-33, and 36 have been canceled in the interest of expediting prosecution. Claims 3, 14-21, and 34 were previously canceled.

The Office Action states that claims 5, 22-29, and 31-33 are withdrawn from consideration as drawn to a non-elected invention and requires that they be canceled or that other appropriate action be taken. Claims 22-29 and 31-33 have been canceled, reserving the right to prosecute them in a divisional application. Claim 5 is dependent from claim 30, which, as set forth below, is allowable, and so claim 5 is likewise allowable.

Claims 1, 6-9, 13, 30, 35, 37, and 38 were rejected under 35 U.S.C. §102(e) as being anticipated by Komada, Patent Application Publication No. 2002/0125577. Claims 11-12 were rejected under 35 U.S.C. §103 as being unpatentable over Komada in view of Ibnabdeljalil, et al., Patent Application Publication No. 2002/0024115. These rejections are respectfully traversed.

In the claimed invention, at least two seal rings are formed upwardly or downwardly through the plurality of wiring insulating films, along a periphery of the semiconductor chip, in such a manner as to surround a specified region on the semiconductor substrate. The seal rings include an outer seal ring surrounding an inner seal ring.

As a consequence, referring to the exemplary embodiment depicted in Figure 1, even

if the first seal ring 20, nearest the dicing face 20 is subjected to corrosion and contamination by water or the like which penetrates through the dicing face, the water is inhibited or blocked from penetrating more deeply into the chip by the second seal ring 22 or a third seal ring 23. This protects the circuit formation portion from corrosion and contamination. See the specification at, for example, page 29, lines 9-16 and page 33, lines 9-20.

Further, in the claimed invention the plurality of seal rings are connected to a diffusion region formed in the semiconductor substrate. If, for example, the seal rings are exposed to plasma in the process of etching, CVD, or the like, ions having a positive charge are likely to hit the semiconductor substrate. The seal rings may be deprived of their inner electrons by the ions, thereby causing the wiring layers to have a positive charge. In such case, as depicted in Figure 4A of the drawings, since the conventional seal ring is in an electrically floating state, it continues to accumulate charge until the charge is discharged, whereupon the substrate may be destroyed.

In contrast, in the present invention, as can be seen from Figures 2 and 4B, each of the seal rings is connected via a contact to the diffusion region, so that the charge on the seal ring is discharged through the semiconductor substrate, preventing destruction of the semiconductor substrate. See the specification at, for example, page 28, line 24 to page 29, line 8.

Komada fails to disclose or suggest a semiconductor chip provided with at least two seal rings, or with a single seal ring connected to a diffusion region formed in the semiconductor substrate. Ibnabdeljalil discloses a plurality of seal rings, but does not disclose or suggest that the seal rings be connected to a diffusion region formed in the semiconductor

substrate. Ibnabdeljalil discloses only that the via groove closest to the semiconductor substrate may be in electrical contact with a heavily doped region of the semiconductor substrate. See paragraph 49 of Ibnabdeljalil.

The cited references, whether considered separately or in combination, thus do not disclose or suggest the claimed invention.

In view of the foregoing, Applicant submits that claims 1, 5-9, 11-13, 30, 35, 37, and 38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

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